

AMENDMENTS

In the Specification

At the beginning of the specification, please insert the following paragraph:

– This application is a continuation of co-pending U.S. Application Serial No. 10/114,463
filed April 3, 2002. –

In the Claims

Please **CANCEL** claims 1-17 without any prejudice and disclaimer and add the
following claims 18-19.

The following is a complete list of all claims in this application.

1-17 (Cancelled)

18. (New) A method for manufacturing a thin film transistor, comprising:

forming an amorphous silicon layer and a blocking layer on an insulating
substrate;

forming a photoresist layer having first and second photoresist patterns on the
blocking layer, the first and second photoresist patterns spaced apart from each other;

etching the blocking layer using the first photoresist pattern as a mask to form
first and second blocking patterns;

reflowing the photoresist layer, so that the first and second photoresist patterns
abut each other to entirely cover the first and second blocking patterns;

forming a metal layer over an entire first surface of the insulating substrate;

removing the photoresist layer to expose the blocking layer and an offset region between the blocking layer and the metal layer;

crystallizing the amorphous silicon layer to form a poly silicon layer with a metal induced lateral crystallization front;

etching the poly silicon layer using the first and second blocking patterns as a mask to form first and second semiconductor layers and to remove the metal induced lateral crystallization front;

removing the first and second blocking patterns; and

forming a metal layer for a source electrode and a drain electrode.

19. (New) A method for manufacturing a thin film transistor, comprising:

forming an amorphous silicon layer on an insulating substrate;

forming a first photoresist layer on the amorphous silicon layer while exposing edge portions of the amorphous silicon layer;

forming a metal layer over an entire first surface of the insulating substrate;

removing the first photoresist layer to expose a portion of the amorphous silicon layer under the first photoresist layer;

crystallizing the amorphous silicon layer to form a poly silicon layer with a metal induced lateral crystallization front;

forming a second photoresist layer having first and second photoresist patterns on the metal induced lateral crystallization front of the poly silicon layer to expose the metal induced lateral crystallization front, the first and second photoresist patterns spaced apart from each other;

etching the poly silicon layer using the first and second photoresist patters as a mask to form first and second semiconductor layers and to remove the metal induced lateral crystallization front;

removing the first and second photoresist patterns; and

forming a metal layer for a source electrode and a drain electrode.